AMIS-30522
Micro-Stepping Motor Driver

1.0 Introduction

The AMIS-30522 is a micro-stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. AMIS-30522 contains a current-translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin. The chip provides a so-called "speed and load angle" output. This allows the creation of stall detection algorithms and control loops based on load-angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS-30522 is implemented in I2T100 technology, enabling both high-voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS-30522 is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on-chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

2.0 Key Features

- Dual H-Bridge for 2-phase stepper motors
- Programmable peak-current up to 1.6A using a 5-bit current DAC
- On-chip current translator
- SPI interface
- Speed and load angle output
- Seven step modes from full step up to 32 micro-steps
- Fully integrated current-sense
- PWM current control with automatic selection of fast and slow decay
- Low EMC PWM with selectable voltage slopes
- Active fly-back diodes
- Full output protection and diagnosis
- Thermal warning and shutdown
- Compatible with 5V and 3.3V microcontrollers
- Integrated 5V regulator to supply external microcontroller
- Integrated reset function to reset external microcontroller
- Integrated watchdog function

3.0 Ordering information

Table 1: Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range	Device/Family Specific #1
AMIS30522C5222G	NQFP-32 (7 x 7mm)	Tube/Tray	-40°C to125°C	1600mA
AMIS30522C5222RG	NQFP-32 (7 x 7mm)	Tape & Reel	-40°C to 125°C	1600mA

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4.0 Block Diagram

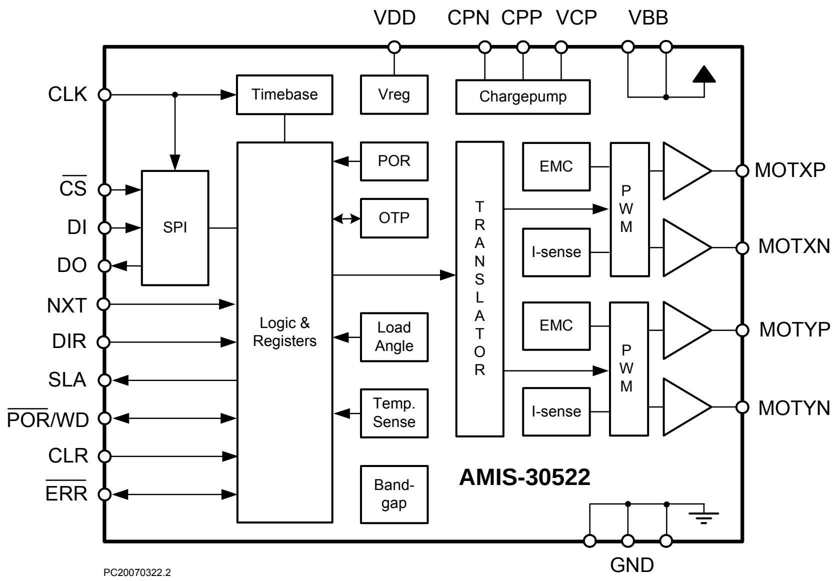

Figure 1: Block Diagram AMIS-30522

5.0 Pin Description

Table 2: Pin List and Description

Name	Pin	Description
DO	31	SPI data output (open drain)
VDD	32	Logic supply output (needs external decoupling capacitor)
GND	1	Ground, heat sink
DI	2	SPI data in
CLK	3	SPI clock input
NXT	4	Next micro-step input
DIR	5	Direction input
ERRB	6	Error output (open drain)
SLA	7	Speed load angle output
CPN	9	Negative connection of charge pump capacitor
CPP	10	Positive connection of charge pump capacitor
VCP	11	Charge pump filter-capacitor
CLR	12	“Clear” = chip reset input
CSB	13	SPI chip select input
VBB	14	High voltage supply Input
MOTYP	15, 16	Negative end of phase Y coil output
GND	17, 18	Ground, heat sink
MOTYN	19, 20	Positive end of phase Y coil output
MOTXN	21, 22	Positive end of phase X coil output
GND	23, 24	Ground, heat sink
MOTXP	25, 26	Negative end of phase X coil output
VBB	27	High voltage supply input
/	8, 30	No function (to be left open in normal operation)
PORB/WD	28	Power-on-reset (POR)and watchdog reset output (open drain)
TSTO	29	Test pin input (to be tied to ground in normal operation)

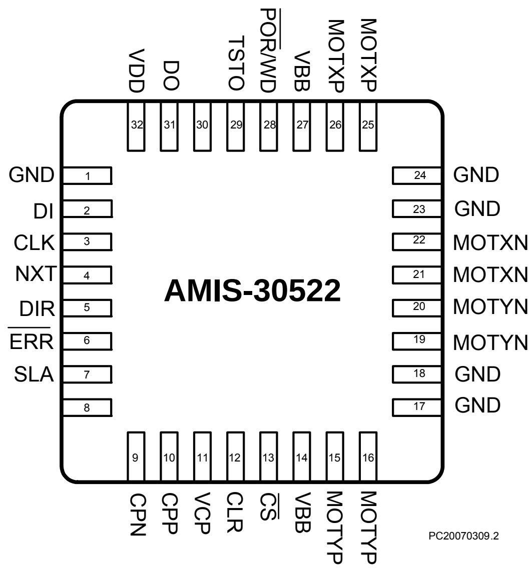

Figure 2: Pin Out AMIS-30522

5.1 Package Thermal Characteristics

The NQFP is designed to provide superior thermal performance, and using an exposed die pad on the bottom surface of the package partly contributes to this. In order to take full advantage of this thermal performance, the PCB must have features to conduct heat away from the package. A thermal grounded pad with thermal via's can achieve this. With a layout as shown in Figure 3, the thermal resistance junction – to – ambient can be brought down to a level of 30°C/W.

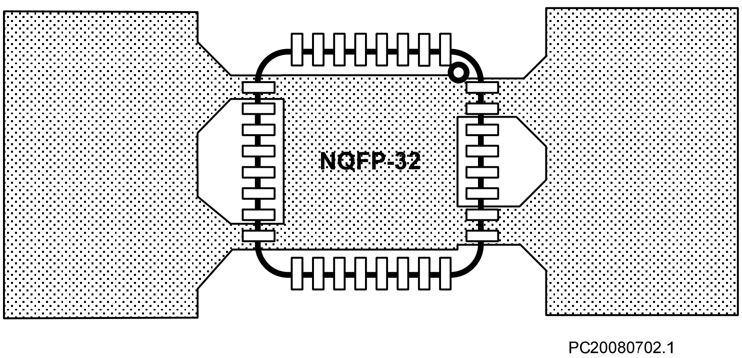

Figure 3: PCB Ground Plane Layout Condition

6.0 Electrical Specification

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 3 may cause immediate and permanent device failure. It is not implied that more that one of these conditions can be applied simultaneously.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{BB}	Analog DC supply voltage (1)	-0.3	+40	V
Tstrg	Storage temperature	-55	+160	°C
Tamb	Ambient temperature under bias	-50	+150	°C
V_{ESD}	Electrostatic discharges on component level (2)	-2	+2	kV

Notes:
(1) For limited time <0.5s.
(2) Human body model (100pF via 1.5 kΩ, according to JEDEC EIA-JESD22-A114-B).

6.2 Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4: Operating Ranges

Symbol	Parameter	Min.	Max.	Units
V_{BB}	Analog DC supply	+6	+30	V
V_{DD}	Logic supply output voltage (1)	4.75	5.25	V
Iddd	Dynamic current of VDD pin (internal and external loads) (2)		18	mA
T_a	Ambient temperature VBAT≤+18	-40	+125	°C
T_a	Ambient temperature VBAT≤+29	-40	+85	°C
T_j	Junction temperature		+160	°C

Notes:
(1) Voltage output.
(2) Dynamic current is with oscillator running, all analog cells active. All outputs unloaded, no floating inputs.

6.3 DC Parameters

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Table 5: DC parameters

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Supply & Voltage Regulator							
V_{BB}	VBB	Nominal operating supply range		6		30	V
I_{BB}		Total internal current consumption	Unloaded outputs			8	mA
V_{DD}	VDD	Regulated Output Voltage		4.75	5	5.25	V
I_{INT}		Internal load current	Unloaded outputs				
I_{LOAD}		Max. Output Current (external and internal loads)	6V < V_{BB} < 8V	20			
			8V < V_{BB} < 30V	50			
I_{DDLIM}		Current limitation	Pin shorted to ground			150	mA
I_{LOAD_PD}		Output current in Power Down		1			
Power-on-Reset (POR)							
V_{DDH}	VDD	Internal POR comparator threshold	VDD rising	4.0	4.25	4.4	V
V_{DDL}		Internal POR comparator threshold	VDD falling		3.68		V
Motor Driver							
$I_{MDmax,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation			1600		mA
$I_{MDmax,RMS}$		Max RMS current through coil in normal operation			800		mA
I_{MDabs}		Absolute error on coil current		-10		10	%
I_{MDrel}		Error on current ratio I_{coilx} / I_{coily}		-7		7	%
I_{SET_TC1}		Temperature coefficient of coil current set-level, CUR[4:0] = 0 ..27	-40 °C ≤ T_j ≤ 160 °C		-240		ppm/K
I_{SET_TC2}		Temperature coefficient of coil current set-level, CUR[4:0] = 28 ..31	-40 °C ≤ T_j ≤ 160 °C		-490		ppm/K
R_{HS}		On-resistance high-side driver, CUR[4:0] = 0...31	V_{bb} = 12V, T_j = 27 °C		0.45	0.56	Ω
			V_{bb} = 12V, T_j = 160 °C		0.94	1.25	Ω
R_{LS3}		On-resistance low-side driver, CUR[4:0] = 23...31	V_{bb} = 12V, T_j = 27 °C		0.45	0.56	Ω
			V_{bb} = 12V, T_j = 160 °C		0.94	1.25	Ω
R_{LS2}		On-resistance low-side driver, CUR[4:0] = 16...22	V_{bb} = 12V, T_j = 27 °C		0.90	1.2	Ω
			V_{bb} = 12V, T_j = 160 °C		1.9	2.5	Ω
R_{LS1}		On-resistance low-side driver, CUR[4:0] = 9...15	V_{bb} = 12V, T_j = 27 °C		1.8	2.3	Ω
			V_{bb} = 12V, T_j = 160 °C		3.8	5.0	Ω
R_{LS0}		On-resistance low-side driver, CUR[4:0] = 0...8	V_{bb} = 12V, T_j = 27 °C		3.6	4.5	Ω
			V_{bb} = 12V, T_j = 160 °C		7.5	10	Ω
I_{Mpd}		Pull down current	HiZ mode		0.5		mA
Digital Inputs							
I_{leak}	DI, CLK NXT, DIR CLR, CSB	Input Leakage (3)	Tj = 160 °C			1	µA
V_{IL}		Logic Low Threshold		0		0.65	V
V_{IH}		Logic High Threshold		2.20		V_{DD}	V
R_{pd_CLR}	CLR	Internal Pull Down Resistor		120		300	kΩ
R_{pd_TST}	TST0	Internal Pull Down Resistor		3		9	kΩ
Digital Outputs							
V_{OL}	DO, ERRB, PORB/WD	Logic Low level open drain	IOL = 5 mA			0.5	V
Thermal Warning & Shutdown							
T_{tw}		Thermal Warning		138	145	152	°C
T_{tsd}(1) (2)		Thermal shutdown			T_{tw} + 20		°C
Charge Pump							
V_{cp}	VCP	Output voltage	6V< V_{BB} < 15V		2 * V_{BB} – 2.5		V
			15V < V_{BB} < 30V	V_{BB}+12.5	V_{BB}+14	V_{BB}+15.5	V
C_{buffer}		External buffer capacitor		180	220	470	nF
C_{pump}	CPP CPN	External pump capacitor		180	220	470	nF

Notes:

(1) No more than 100 cumulated hours in life time above Tt_w.

(2) Thermal shutdown and low temperature warning are derived from thermal warning.

(3) Not valid for pins with internal pull-down resistor.

6.4 AC Parameters

The AC parameters are given for V_{BB} and temperature in their operating ranges.

Table 6: AC Parameters

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min.	Typ.	Max.	Unit
Internal Oscillator							
f_{osc}		Frequency of internal oscillator		3.6	4	4.4	MHz
Motor Driver							
f_{PWM}	MOTxx	PWM frequency	Frequency depends only on internal oscillator	20.8	22.8	24.8	kHz
		Double PWM frequency		41.6	45.6	49.6	kHz
f_j		PWM jitter frequency			tbd		Hz
f_d		PWM jitter Depth			tbd		% f_{PWM}
Tb_{rise}	MOTxx	Turn-on voltage slope, 10% to 90%	EMC[1:0] = 00		150		V/µs
			EMC[1:0] = 01		100		V/µs
			EMC[1:0] = 10		50		V/µs
			EMC[1:0] = 11		25		V/µs
Tb_{fall}	MOTxx	Turn-off voltage slope, 90% to 10%	EMC[1:0] = 00		150		V/µs
			EMC[1:0] = 01		100		V/µs
			EMC[1:0] = 10		50		V/µs
			EMC[1:0] = 11		25		V/µs
Digital Outputs							
T_{H2L}	DO ERRB	Output fall-time from V_{inH} to V_{inL}	Capacitive load 400pF and pull-up resistor of 1.5 kΩ			50	ns
Charge Pump							
f_{CP}	CPN CPP	Charge pump frequency			250		kHz
T_{CPU}	MOTxx	Start-up time of charge pump	Spec external components				
CLR Function							
T_{CLR}	CLR	Hard reset duration time		20		90	µs
Power-Up							
t_{PU}	PORB/ WD	Power-up time	V_{BB}=12V, I_{LOAD}=50mA, C_{LOAD}=220nF			110	µs
t_{PD}		Power-down time	External conditions tbd				ms
t_{POR}		Reset duration			100		ms
t_{RF}		Reset filter time			1		µs
Watchdog							
t_{WDTO}	PORB/ WD	Watchdog time out interval		32		512	ms
t_{WDPR}		Prohibited watchdog acknowledge delay			2		ms
t_{WDRD}		Watchdog reset delay			tbd		µs

6.5 SPI Timing

Table 7: SPI Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	SPI clock period	1			µs
t_{CLK_HIGH}	SPI clock high time	100			ns
t_{CLK_LOW}	SPI clock low time	100			ns
t_{SET_DI}	DI set up time, valid data before rising edge of CLK	50			ns
t_{HOLD_DI}	DI hold time, hold data after rising edge of CLK	50			ns
t_{CSB_HIGH}	CSB high time	2.5			µs
t_{SET_CSB}	CSB set up time, CSB low before rising edge of CLK	100			ns
t_{SET_CLK}	CLK set up time, CLK low before rising edge of CSB	100			ns

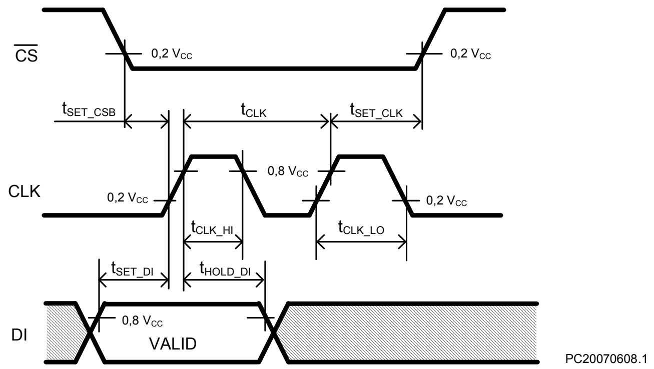

Figure 4: SPI Timing

7.0 Typical Application Schematic

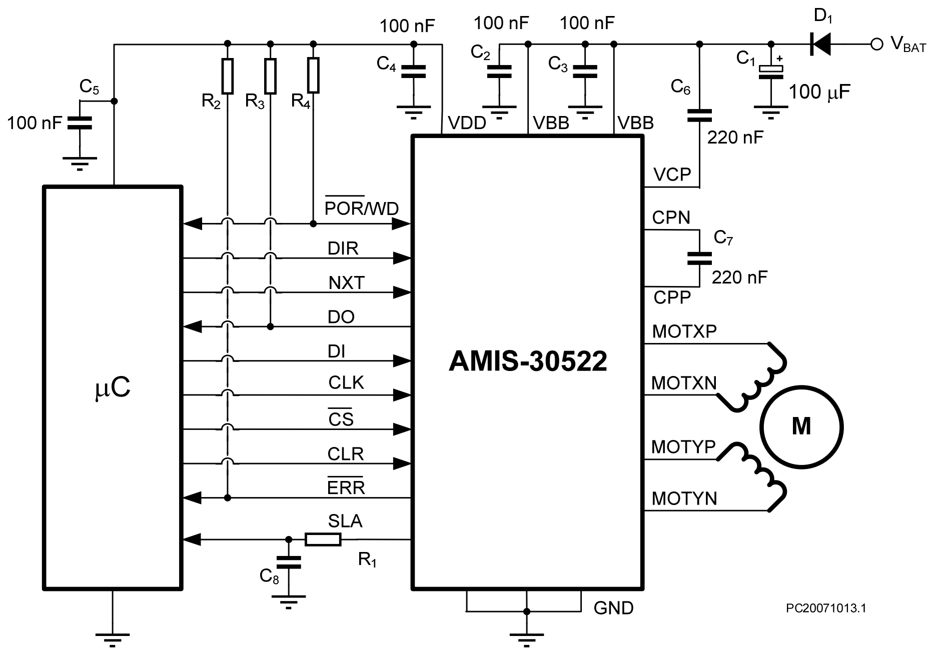

Figure 5: Typical Application Schematic AMIS-30522

Table 8: External Components List and Description

Component	Function	Typ. Value	Tolerance	Unit
C_1	V_{BB} buffer capacitor (1)	100	-20 +80%	µF
C_2, C_3	V_{BB} decoupling block capacitor	100	-20 +80%	nF
C_4	V_{DD} buffer capacitor	220	+/- 20 %	nF
C_5	V_{DD} buffer capacitor	100	+/- 20%	nF
C_6	Charge-pump buffer capacitor	220	+/- 20%	nF
C_7	Charge-pump pumping capacitor	220	+/- 20%	nF
C_8	Low pass filter SLA	1	+/- 20%	nF
R_1	Low pass filter SLA	5.6	+/- 1%	kΩ
R_2, R_3, R_4	Pull up resistor open drain output	4,7	+/- 1%	kΩ
D_1	Optional reverse protection diode	e.g. 1N4003		

Notes:

1. Low ESR < 1Ohm.

8.0 Functional Description

8.1 H-Bridge Drivers

A full H-bridge is integrated for each of the two stator windings. Each H-bridge consists of two low-side and two high-side N-type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high-impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H-bridge switches, it is guaranteed that the top- and bottom-switches of the same half-bridge are never conductive simultaneously (interlock delay).

A two-stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate-drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see Table 27).

The power transistors are equipped with so-called “active diodes”: when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain-bulk diode of the transistor.

Depending on the desired current range and the micro-step position at hand, the Rdson of the low-side transistors will be adapted such that excellent current-sense accuracy is maintained. The Rdson of the high-side transistors remain unchanged, see **Error! Reference source not found.** for more details.

8.2 PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H-bridge switches. The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see Table 16). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

8.2.1. Automatic Forward and Slow-Fast Decay

The PWM generation is in steady-state using a combination of forward and slow-decay. The absence of fast-decay in this mode, guarantees the lowest possible current-ripple “by design”. For transients to lower current levels, fast-decay is automatically activated to allow high-speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

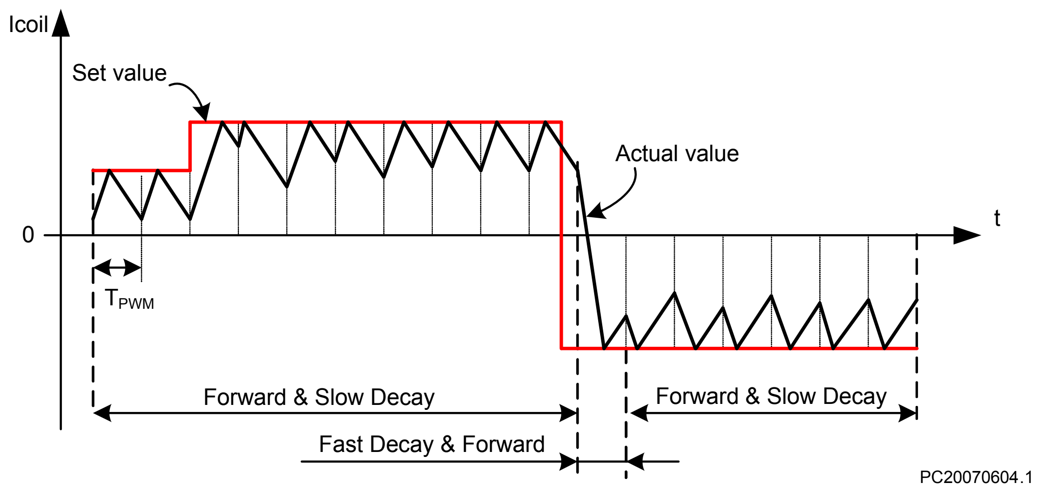

Figure 6: Forward and Slow/Fast Decay PWM

8.2.2. Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to >50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over-all current-ripple is divided by two if PWM frequency is doubled (see Table 16).

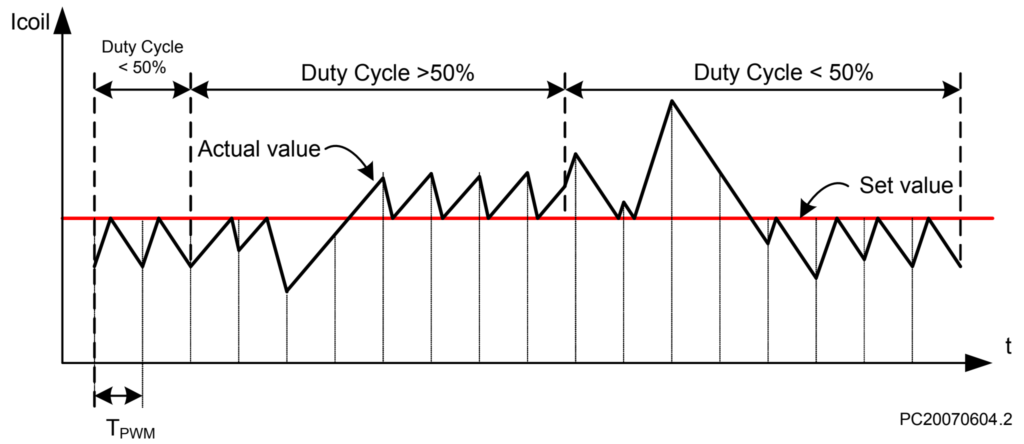

Figure 7: Automatic Duty Cycle Adaptation

8.3 Step Translator

8.3.1. Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL, and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI-bits SM[2:0] (see Table 28) After power-on or hard reset, the coil-current translator is set to the default 1/32 micro-stepping at position **'0'**. Upon changing the step mode, the translator jumps to position **0*** of the corresponding stepping mode. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. **Error! Reference source not found.** lists the output current vs. the translator position.

As shown in Figure 8 the output current-pairs can be projected approximately on a circle in the (I_x,I_y) plane. There is, however, one exception: uncompensated half step. In this step mode the currents are not regulated to a fraction of Imax but are in all intermediate steps regulated at 100 percent. In the (I_x,I_y) plane the current-pairs are projected on a square. **Error! Reference source not found.** lists the output current vs. the translator position for this case.

Table 9: Square Translator Table for Full Step and Uncompensated Half Step

MSP[6:0]	Stepmode (SM[2:0])		% of Imax	
	101	110	Coil x	Coil y
	Uncompensated Half-Step	Full Step		
000 0000	**0***	-	0	100
001 0000	1	1	100	100
010 0000	2	-	100	0
011 0000	3	2	100	-100
100 0000	4	-	0	-100
101 0000	5	3	-100	-100
110 0000	6	-	-100	0
111 0000	7	**0***	-100	100