Flexible Memory Controller (FMC)

Enhanced and upgrade of FSMC
CONTENTS

• FMC features
• SDRAM protocol
• SDRAM FMC controller
OBJECTIVES

• Overview of FMC interface

• Usage of high capacity RAM storage - SDRAM
  • For frame buffer
  • For picture storage and preparation
  • For animations
FMC Features (1/2)

• 6 Banks to support External memories
• FMC external access frequency is up 90MHz when HCLK is at 180MHz
• Independent chip select control for each memory bank
• Independent configuration for each memory bank
• Programmable timings to support a wide range of devices
• 8/16/32 bits data bus
• External asynchronous wait control
• Interfaces with Synchronous DRAM (SDRAM) memory-mapped
FMC Features (2/2)

• Interfaces with static memory-mapped devices including:
  • static random access memory (SRAM)
  • read-only memory (ROM)
  • NOR/OneNAND Flash memory
  • PSRAM

• Interfaces parallel LCD modules: Intel 8080 and Motorola 6800

• Interfaces with NAND Flash and 16-bit PC Cards
  • With ECC hardware up to 8 Kbyte for NAND memory
  • 3 possible interrupt sources (Level, Rising edge and falling edge)

• Supports burst mode access to synchronous devices (NOR Flash and PSRAM)
SDR SDRAM protocol overview
SDRAM memory organization

- Example of DRAM array with 12-bits row and 10-bits column
  - A row width is $2^{10} = 1024$ column
  - Column width is 8-bit, 16-bit or 32-bit ($C_w$)

Row width : 1024 columns

Row Buffer

Column decoder

Memory interface

8-/16- or 32-bits Data Returned to MCU, one per cycle
SDRAM memory read operation

• Read operation step 1(*):
  • On Row Access Strobe (RAS), selected row is copied to “Row Buffer” (a full row is transferred at once to the Row Buffer)

• Read operation step 2:
  • On Column Access Strobe (CAS), column is selected from “Row Buffer” and presented on the memory interface

(*): Row activation is only performed if the row is not active or at a row boundary
SDRAM memory read characteristics

- SDRAM read characteristics
  - Reads are destructive: contents are erased after reading
  - Row buffer
    - read a full row at once (a set of bits all at once), and then break down them based on different column addresses

Diagram:

- Wordline Enabled
- Sense Amp Enabled
- After read cell contains something close to ½ Vdd
- Storage cell voltage
SDRAM memory write characteristics

• The SDRAM controller always checks the next write access destination,

• Two cases:
  • If the next write access is in the same row or in another active row (in a different bank)
    • The write operation is carried out
  • If the next write access targets another row (not active), the SDRAM controller
    • Generates a precharge command
    • Activates the new row
    • Initiates a write command
STM32 FMC controller
FMC SDRAM main features (1/4)

- Up to 512MB continues memory range split into two banks, can be seen as a single device.
SDRAM main features (2/4)

- Fully programmable SDR (single data rate) SDRAM interface
- Configurable SDRAM clock speed
  - Half AHB speed (HCLK /2),
  - One-third AHB speed (HCLK /3)
- Programmable Timing parameters for different SDRAM devices requirements
  - Row to column delay (TRCD)
  - Self refresh time
  - CAS latency of 1,2,3
- Memory data bus width: 8-bit, 16-bit and 32-bit
- Up to 4 internal banks with configurable Row and Column sizes:
  - up to 13-bits Address Row,
  - up to 11-bits Address Column.
SDRAM main features (3/4)

• Optimized initialization sequence by software
  • The initialization command sequence are executed simultaneously for the two banks. Initialization time can be divided by 2.

• Automatic Refresh operation with programmable Refresh rate

• Energy-saving capabilities : two low power modes are supported:
  • Self-refresh Mode
  • Power-down Mode
SDRAM main features (4/4)

• Multibank ping-pong access (FMC SDRAM controller keeps track of the active row in each bank)

• Automatic row and bank boundary management

• Optimized Read access:
  • Cacheable Read FIFO with depth of 6 lines x 32-bit
  • With 6x 14-bit Address Tag to identify each FIFO line content
  • Configurable Read Burst (to anticipate next read accesses during CAS latencies)

• Buffered write access
  • Write Data FIFO with depth of 16
  • With 16x Write Address FIFO to identify each FIFO line destination
SDRAM controller benefits

- AHB Slave interface up to 180MHz
- Grant more RAM resources for user application
- Accessible by all AHB masters
  - CPU can execute code from SDRAM
- Reduce RAM memory cost (SDRAM vs. SRAM)