650 V CoolMOS™ C7 gold and TO-leadless package

Stefan Gamerith
February 2017
Agenda

1. Power density - C7 Gold higher efficiency
2. Power density - kelvin source efficiency benefits
3. Efficiency & thermals in a 3 kW low line PFC circuit
4. Power density - TOLL comparison to D²PAK/TO-220/TO-247
5. SMD manufacturing cost reduction
6. High quality features of CoolMOS™ and TOLL package
7. Portfolio
8. Conclusion
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C7 Gold & TOLL package combination - benefits for both power density and costs

- Higher efficiency from C7 Gold technology
- High efficiency due to low package parasitic inductance
- High efficiency due to 4pin Kelvin Source capability
- Improved thermal performance from TOLL package
- First time ever medium to high power PFC or boost circuits with an SMD device

1. Higher power density
2. Cost reduction
3. High quality & ease-of-use

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Power density
Higher efficiency – lower thermals

C7 Gold again improves performance in high efficiency applications such as server and telecom

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Competitor A</th>
<th>Competitor B</th>
<th>CoolMOS™ C7</th>
<th>CoolMOS™ C7 GOLD (G7)</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>D²PAK</td>
<td>D²PAK</td>
<td>TOLL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Footprint</td>
<td>150 mm²</td>
<td>150 mm²</td>
<td>115mm²</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage (V)</td>
<td>600</td>
<td>650</td>
<td>650</td>
<td>650</td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)} \text{ max. [mΩ]}$</td>
<td>95</td>
<td>95</td>
<td>95</td>
<td>105</td>
<td></td>
</tr>
<tr>
<td>$Q_g \text{ typ [nC]}$</td>
<td>100</td>
<td>71</td>
<td>45</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>$C_{oss} \text{ typ [pF]}$</td>
<td>156</td>
<td>74</td>
<td>33</td>
<td>26</td>
<td></td>
</tr>
</tbody>
</table>

C7 technology already best-in-class over competition

C7 Gold increases again performance
Additional efficiency boost at full load - from innovative TOLL package

Parasitic source inductance counteracts drive voltage

Lower efficiency due to slow down of transient

Separate pin “source-sense” delivers undisturbed signal to driver

Higher efficiency at full load
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Low line efficiency difference -3 kW PFC circuit

Efficiency difference low line

Efficiency increase of TOLL vs. TO-247 comes from
- Lower $R_{DS(on)}$
- 4pin Kelvin Source
Temperature – Thermal measurement

- Lower temperature of TOLL vs TO-247 comes from
  - Increased efficiency (0.6% at full load)
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TOLL a replacement for D²PAK
- Space and inductance

Footprint: 150 mm²

- 30% footprint reduction
- 5 nH inductance
- RthJc 0.98°C/W

Footprint: 115 mm²

- 50% height reduction
- 1 nH inductance
- RthJc 0.8°C/W

- 60% space reduction
Power density - Best $R_{DS(on)}/package$

- CoolMOS™ C7 with the best $R_{DS(on)}$ in the world
- CoolMOS™ C7 Gold is even better

- Infineon already have the best $R_{DS(on)}$ in D²PAK
- Now improved again with C7 GOLD and TOLL package with smaller footprint
Power density
– Package & $R_{DS(on)}$

**TO-247**
- 16.13mm
- 21.1mm
- 20.32mm

**TO-220**
- 10.36mm
- 15.95mm
- 14.0mm

**D²PAK**
- 10 mm
- 15mm

**TOLL**
- 9.9 mm
- 11.7mm

50% footprint reduction

30% footprint reduction

<table>
<thead>
<tr>
<th>Package inductance</th>
<th>15nH</th>
<th>10nH</th>
<th>5nH</th>
<th>1nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoolMOS™ 650 V</td>
<td>IPW65R019C7 19 mΩ</td>
<td>IPP65R045C7 45 mΩ</td>
<td>IPB65R045C7 45 mΩ</td>
<td>IPT65R033G7 33 mΩ</td>
</tr>
</tbody>
</table>
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3. High quality & ease-of-use
System costs
- The voice of the customer

Customer question:
Are there savings in assembly costs from moving from through hole to SMD devices?

- Yes 87%
- No 13%

Quicker assembly saves costs, but using a daughter board for power density may increase them again.

Mount devices in one simple process.

Reduced manual assembly/labor cost.

Quicker assembly time.
Customer question:
Are there cost adders such as PCB vias for cooling when moving to SMD solution?

- No extra cost for the PCB vias
- No significant cost adders seen for PCB vias
- Cost adder may happen for some cases but in general overall SMD approach still has benefits
- PCB vias may add cost. But depends on the power and cooling method
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1. Higher power density
2. Cost reduction
3. High quality & ease-of-use
Highest quality & reliability CoolMOS™
- 38 fails over 1.6 bn shipped parts

38 fails

> 1.6 bn parts shipped

All CoolMOS™ Technologies

› 0.03 DPM on average

› Only 38 fails from 1.6 bn parts shipped
TO-Leadless package
- highest quality

- TOLL package
  - Totally Pb free
  - MSL1 compliant
  - Suitable for wave or reflow soldering

JEDEC Industrial applications qualified (J-STD20 and JESD22)

<table>
<thead>
<tr>
<th>Level</th>
<th>Floor Life (out of bag) at factory</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ambient ≤30°C/60% RH or as stated</td>
</tr>
<tr>
<td>2</td>
<td>1 year</td>
</tr>
<tr>
<td>2a</td>
<td>4 weeks</td>
</tr>
<tr>
<td>3</td>
<td>168 hours</td>
</tr>
<tr>
<td>4</td>
<td>72 hours</td>
</tr>
<tr>
<td>5</td>
<td>48 hours</td>
</tr>
<tr>
<td>5a</td>
<td>24 hours</td>
</tr>
<tr>
<td>6</td>
<td>Mandatory bake before use.</td>
</tr>
</tbody>
</table>

IPC/JEDEC J-STD-033B.1
Table 5-1 Moisture Classification Level and Floor Life

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TO-Leadless - enables possibility of optical inspection

The TO-Leadless packages enables a visual inspection due to Tin plated and grooved leads

 guaranted wetting

Visible solder joint

Pin of TO-Leadless

Groove

Tracks on PCB

PCB
650 V CoolMOS™ C7 Gold TOLL - applications

<table>
<thead>
<tr>
<th>Topologies</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power factor correction (CCM and DCM mode PFC)</td>
<td>▶ Telecom</td>
</tr>
<tr>
<td>TTF &amp; iTTF DC-DC topologies</td>
<td>▶ Server</td>
</tr>
<tr>
<td>High efficiency diode bridge rectifier replacement</td>
<td>▶ Industrial</td>
</tr>
<tr>
<td>Boost topology</td>
<td>▶ Solar</td>
</tr>
</tbody>
</table>
650 V CoolMOS™ C7 Gold TOLL - circuit examples of usage (PFC & Boost)
Demonstrator boards

2.5kW PFC demonstrator board

1 * IPT65R033G7 (TOLL)
1 * IDK12G65C5 (D²PAK)

2.5kW Totem Pole PFC demonstrator board

2 * IGO60R070D1 GaN (DS020)
2 * IPT65R033G7 (TOLL)
C7 Gold (G7) portfolio and availability
- TOLL package

<table>
<thead>
<tr>
<th>R(_{DS(on)}) max. [mΩ]</th>
<th>TOLL G7 650V</th>
<th>TOLL G7 600V</th>
</tr>
</thead>
<tbody>
<tr>
<td>195</td>
<td>IPT65R195G7</td>
<td>150</td>
</tr>
<tr>
<td>105</td>
<td>IPT65R105G7</td>
<td>125</td>
</tr>
<tr>
<td>33</td>
<td>IPT65R033G7</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td></td>
<td>80</td>
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<tr>
<td></td>
<td></td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>28</td>
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**Product release**: May.16

**Samples**: Q4 2016

**Product release**: Q1 2017
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Benefits in combining TOLL and CoolMOS™ C7 Gold technology

<table>
<thead>
<tr>
<th>Technology</th>
<th>Product features</th>
<th>Customer benefits</th>
</tr>
</thead>
</table>
| C7 Gold          | Best-in-class Figure Of Merit  
1. $R_{\text{DS(on)}} \cdot E_{\text{ooss}}$  
2. $R_{\text{DS(on)}} \cdot Q_{\text{g}}$  
World lowest $R_{\text{DS(on)}}$/package | Higher system efficiency by enabling lower switching losses  
Improved performance & power density  
Improved power density over D²PAK and TO-220  
High quality & ease-of-use for manufacturing  
Improved efficiency & ease-of-use  
Can be used in higher current applications |
| TOLL package     | Space reduction vs. D²PAK & TO-220  
1. MSL1 compliant  
2. wave and reflow solderable  
3. visual inspection due to grooved leads  
4 pin capability enables Kelvin Source connection  
low parasitic inductance  
Thermal improvement over D²PAK and similar to TO-220 |  

1st SMD device for up to 3kW PFC

* TOLL will also be a package of choice for new CoolGaN™ products

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Support material

Collaterals and Brochures
- Product Briefs
- Selection Guides
- Application Brochures
- Presentations
- Press Releases, Ads

Technical Material
- Application Notes
- Technical Articles
- Simulation Models
- Datasheets, MCDS Files
- PCB Design Data

Videos
- Technical Videos
- Product Information Videos

Contact
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