AN5042
Application note

HSE trimming for RF applications using the STM32WB Series

Introduction

This application note describes the HSE trimming for RF applications using any device of the STM32WB Series.

The STM32WB Series microcontrollers offer a cost-effective and efficient solution by using their internal load capacitances to control the oscillator accuracy, hence saving the cost of external capacitances and lowering the crystal constraints.

These devices use an external oscillator high-speed clock source as the base for RF clock generation. HSE accuracy is essential for RF system performance and the external oscillator is therefore fine-tuned to achieve the highest clock accuracy.

The first part of this application note introduces the STM32WB crystal oscillator solution. The second part presents an example of HSE tuning procedure based on the STM32WB-Nucleo board.

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The RF systems require high frequency accuracy to achieve the best performance. Any clock deviation can cause the system malfunction and/or poor performance.

Table 1 shows the accuracy requirements for two RF protocols supported by microcontrollers of the STM32WB Series, based on Arm®(a) Cortex® cores.

Table 1. Carrier accuracy requirement for RF protocols

RF standard	Carrier accuracy
Bluetooth® Low Energy	± 20 ppm
IEEE 802.15.4 / Thread	± 40 ppm

In the STM32WB Series, the RF clock is provided by a high frequency VCO, which takes as reference a signal created by an embedded oscillator using an external crystal.

This crystal is the HSE (High-Speed External) clock source of the RF synthesizer and microcontroller. Its nominal frequency of 32 MHz can however vary, depending on various factors such as process variation, used crystal and PCB design. Since this inaccuracy of the HSE is directly transferred to the RF clock (in ppm), it must be fine-tuned for each board by adjusting load capacitance at crystal terminals.

STM32WB Series offers an efficient architecture with internal load capacitances that allow the users to fine tune the crystal frequency without extra cost for additional external capacitances.

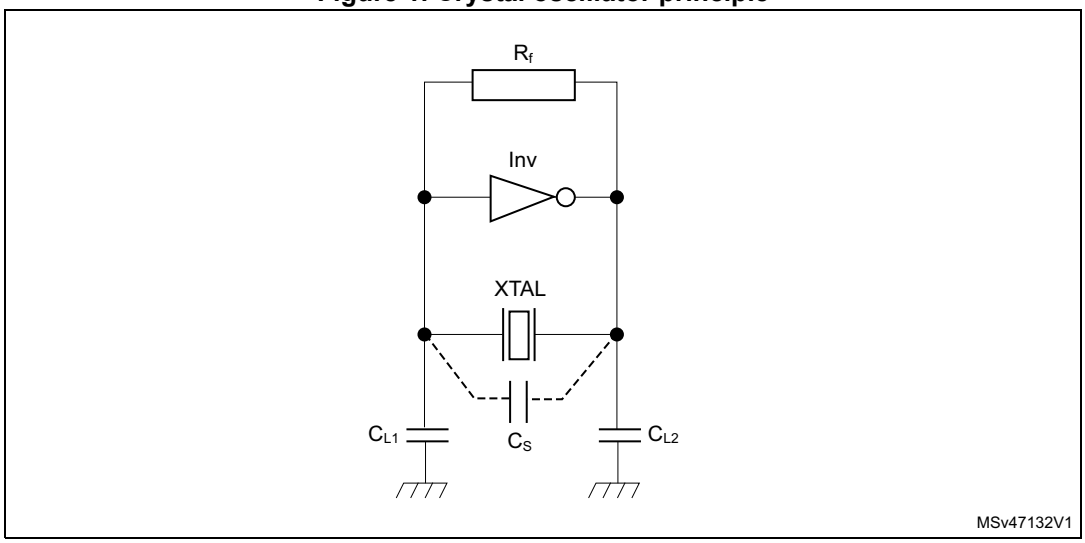
Note: AN2867 (Oscillator design guide for ST microcontrollers), which generally describes HSE for STM32 product, does not apply to STM32WB Series due to the RF constraints. This application note replaces it.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Crystal oscillator

Figure 1 shows the crystal oscillator system principle. An oscillator consists of an inverting amplifier, a feedback resistor (R_f), the crystal itself (XTAL) and two load capacitors C_{L1} and C_{L2}. C_s is the stray capacitance, addition of the MCU pin capacitances (OSC_IN and OSC_OUT) and the PCB capacitance: it is a parasitic capacitance.

Figure 1. Crystal oscillator principle



C_L load capacitance

The load capacitance is the terminal capacitance of the circuit connected to the crystal oscillator. This value is determined by the external capacitors C_{L1} and C_{L2} and the stray capacitance of the printed circuit board and connections (C_s). The C_L value is specified by the crystal manufacturer. For the frequency to be accurate, the oscillator circuit has to show the same load capacitance to the crystal as the one the crystal was adjusted for.

Frequency stability mainly requires that the load capacitance be constant. The external trimming capacitors C_{L1} and C_{L2} are used to tune the desired value of C_L to reach the value specified by the crystal manufacturer.

The following equation gives the expression of C_L

Equation 1: Load capacitance

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

1.2 STM32WB Series architecture

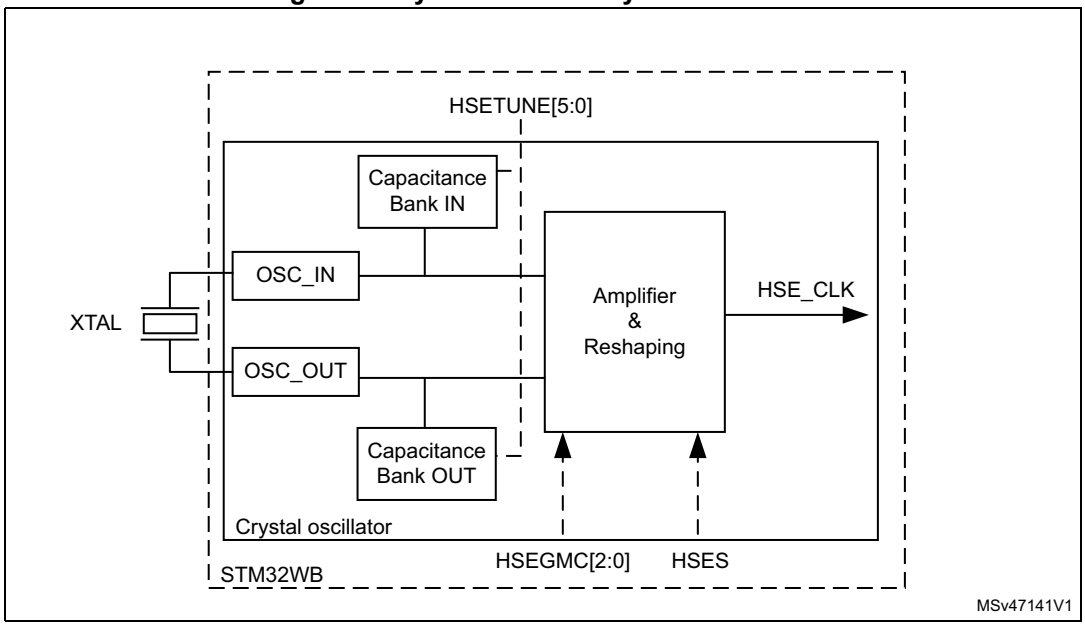
STM32WB Series embeds an efficient and cost-effective crystal oscillator system with internal capacitances for trimming. The advantages of internal mechanism for load capacitance tuning are twofold:

- it reduces the accuracy constraints on the external crystal
- It reduces the global BOM (and the footprint) of the PCB.

Figure 2 shows the crystal oscillator system embedded in the STM32WB Series.

The crystal is the only part of the system to be external. No extra load capacitance are needed.

Figure 2. Crystal oscillator system overview



The crystal oscillator system consists of two pads (OSC_IN and OSC_OUT) with their respective capacitance banks, and the amplifier stage. Three parameters, driven by register, control the system behavior. These parameters are explained in *Section 1.3*.

1.3 HSE configuration parameters

Three parameters can be set to control oscillator module. They are accessible in the RCC_HSECR register described below:

RCC_HSECR

Address offset:

Reset value: 0x0000 0030

Address	0x09C
Reset	0x0000 0030
Access	This register is protected to avoid on-the-fly modification. A key (0xCAFECAFE) shall be written at the register address to unlock it before any single write access. It is then locked again. The HSE clock shall be switch off during register access procedure to avoid unpredictable behavior(1).

1. Note that HSE shall not be used as CPU clock source during this step. In this AN, the default MSI clock is used as system clock source after startup from Reset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	HSETUNE[5:0]						Res.	HSEGMC[2:0]			HSES	Res.	Res.	UNLOCKED
		rw	rw	rw	rw	rw	rw		rw	rw	rw	rw			rw

Load capacitance: HSETUNE[5:0]

This is the parameter responsible for the clock accuracy. It selects the capacitance value added on both input and output pads. The adjustable range is so that the global load capacitance is between 12 and 16 pf. Minimum value (0x00) corresponds to the smallest load capacitance.

Default value is 0x00 (minimum load capacitance).

Current control: HSEGMC[2:0]

This parameter is the transfer conductance of the amplifier. It controls the startup performances of the system. A low value will decrease the power consumption while a high value will improve the startup time.

Minimum values (0b000) correspond to a current limit of 0.18 mA/V; maximum value (0b111) to a current limit of 2.84 mA/V. Default value is 0x3 (current max limit 1.13 mA/V).

HSES sense amplifier threshold

This parameter controls an internal comparison threshold for the oscillator startup. When this bit is set (1), the startup time is reduced (from around 15 µs) but the current consumption is higher.

Default value is 0x0 (1/2 ratio).

1.4 Board implementation

Oscillator pads are available on different pins depending to the package. *Table 2* shows the pin number with three different packages used in Nucleo and USB dongle boards.

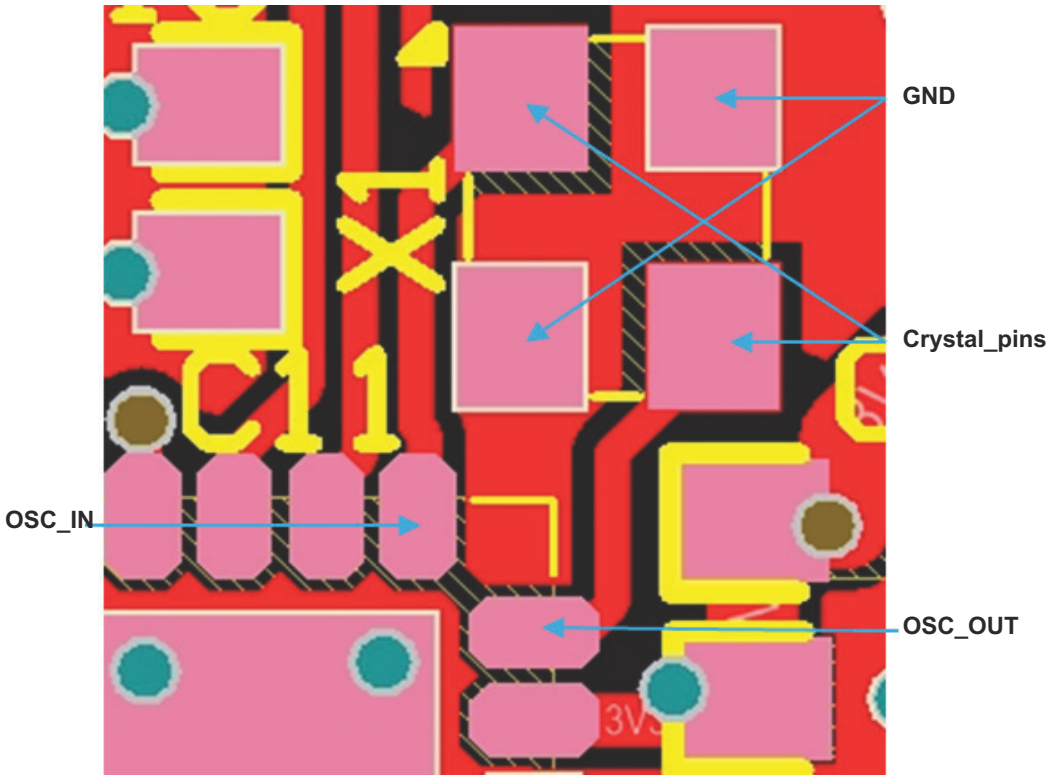
Table 2. Oscillator pin number for UFQFPN48, VFQFPN68 and WLCSP100 packages

Package	OSC_IN	OSC_OUT
UFQFPN48	25	24
VFQFPN68	35	34
WLCSP100	J1	J2

The crystal is plugged directly to the pads, with no extra capacitance, and as close as possible to the device to minimize parasitic capacitance.

Figure 3 shows a typical UFQFPN48 footprint.

Figure 3. UFQFPN48 (USB Dongle board) footprint detail



Crystal reference

Table 3 shows the specification of NDK crystal (NX2016SA 32 MHz EXS00A-CS06654), used to validate the reference designs.

Table 3. Crystal specifications

Component	Value
Load capacitance	8 pF
Frequency tolerance	(25 ± 3 °C) ± 10 × 10^{-6}
Frequency versus temperature characteristics (with reference to +25 °C)	± 25 × 10^{-6}

2 Trimming procedure example

The firmware associated to this application note is available as a software expansion for STM32Cube.

2.1 Procedure description

The procedure consists in measuring the HSE clock generated inside the device from the external crystal. This clock is output on pin PA8 and is measured by a precision frequency-meter.

Note: An external reference is mandatory since no such accurate internal one exists in the device.

A step-by-step tuning of the load capacitance is performed to reach the best accuracy of the HSE clock. The load capacitance value is then stored inside a non-volatile location of the device, either a dedicated area of the user Flash memory or in the One-Time-Programming area.

Flash memory or OTP programming is done with a double-word granularity (64 bits). In order to save OTP bytes (1 K in the STM32WB Series), the load capacitance value on 6 bits can be appended to a 64-bit wide structure with other personalization data (such as the Bluetooth® device address, the MAC short address, the product specific code, the key).

This procedure can be done several times, only the latest setup will be active.

Once the procedure is completed, the active load capacitance value can be retrieved at startup (in the clock configuration function) and the HSE configuration register set accordingly.

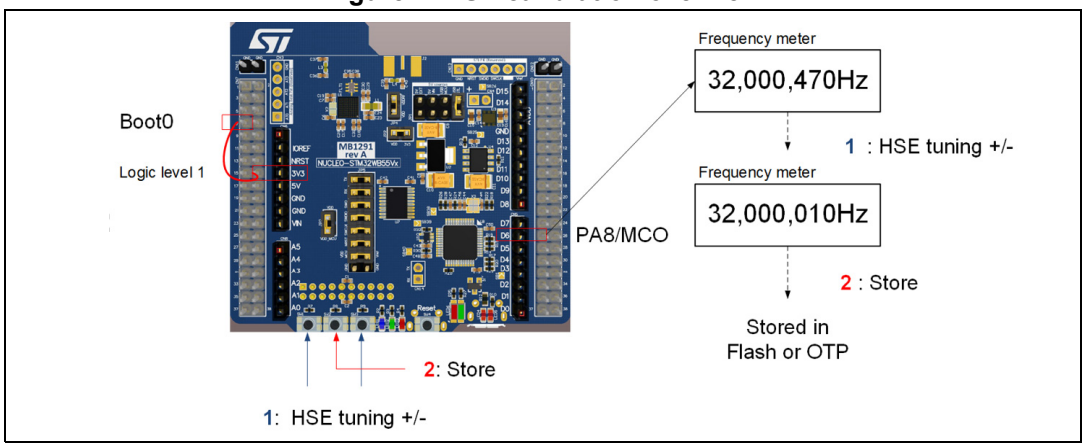
2.2 Implementation

The procedure will be executed in SRAM, so it can be executed on an already programmed device without modifying the Flash memory content.

2.2.1 Hardware setup

Figure 4 shows the HSE calibration procedure for a STM32WB Series Nucleo-68 board.

Figure 4. HSE calibration overview



A precision frequency meter (better than 0.1 ppm) must be connected to pin PA8/MCO and it must be set to detect a 32 MHz 3.3 V square wave peak to peak signal.

Note: Standard oscilloscope does not give enough accuracy to be used in this kind of measurement.

Boot from SRAM

Boot selection can be done through the BOOT0 pin and nBOOT1 bit in the User options (FLASH_OPTR). The boot from SRAM configuration is set by both Boot0=1 and nBoot1=0 conditions. nBoot1 is set only by option bit FLASH_OPTR[23]. Boot0 can be selected either by:

- Through value of pin PH3 at startup if option bit nSWBOOT0 is 1 (FLASH_OPTR[26]=1). See the option byte panel in Figure 2 2.
- Through option bit value nBOOT0 if option bit nSWBOOT0 is 0 (FLASH_OPTR[26]=0). See the option byte panel in Figure 2 3.

Option bits can be selected through ST-Link Utility.

Figure 5. OB configuration to boot from SRAM with BOOT0 value driven by PH3 pin

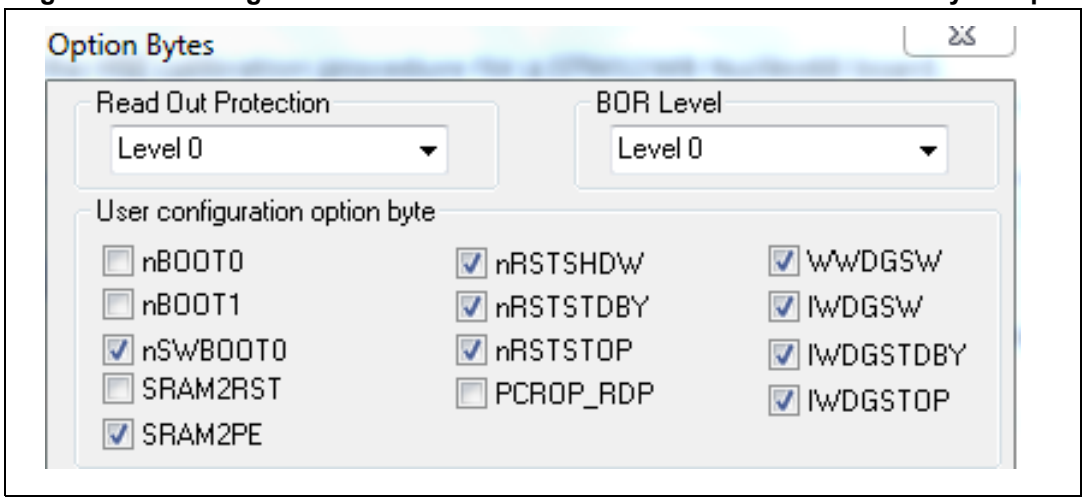
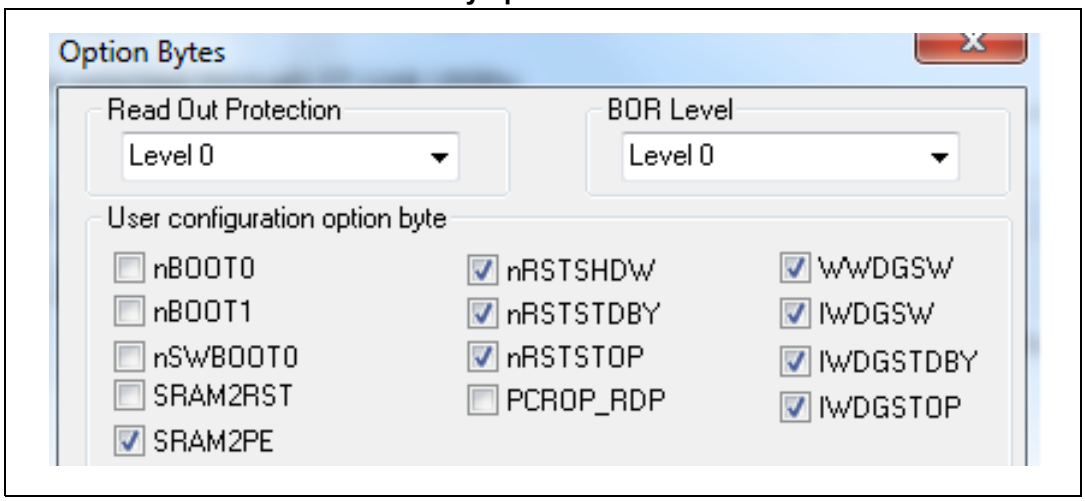


Figure 6. OB configuration to boot from SRAM with BOOT0 value driven by option bit nBOOT0



Clock output

HSE clock is output on the pin PA8 (MCO), which is available on connectors CN9/D6 and CN10/25. PA8 configuration is performed in the firmware. Frequency meter probe is connected to one of these connectors and ground can be taken from connector CN11 or CN12. According with the type of frequency meter used, it can be needed to use AC coupling instead of DC.

The next sequence is required to output the HSE on the MCO pin.

1. Turn on the HSE oscillator:
   a) Set clock control register RCC_CR[16]=1
2. Configure PA8 pin to Clock Output function
   a) Select GPIO alternate function to MCO (= 0x0)
   b) Select GPIO speed to Very High Frequency (= 0x3)
3. Select HSE as output clock with no division factor:
   a) Clock configuration register RCC_CFGR[30:24] = 0b000_0100

Load capacitance setting

The RCC_HSECR[13:8] register drives the load capacitance.

The proposed procedure uses the three push-button available on the Nucleo68 board to modify the register value:

- Pushing SW1 button increases this value by 1.
- Pushing SW3 button is decreasing it by 1.
  – Initial value is set to 0 after reset, it cannot be increased above 0x3F (maximum load capacitance) and cannot be decreased below 0x0 (minimum load capacitance). After each action, the frequency has to be measured.

The next sequence is required for each tested value:

1. Disable the HSE clock:
   – Clock control register RCC_CR[16]=0
2. Unlock RCC_HSECR register:
   – WRITE_REG(RCC_HSECR, 0xCAFECAFE);
3. Write the 6 bits of load capacitance in RCC_HSECR[13:8]
4. Turn on the HSE oscillator:
   – Clock control register RCC_CR[16]=1

Other fields of the register remain unchanged in this procedure and keep their initial value:

- HSE current control (HSEGMC = RCC_HSECR[6:4]) is set to 0x3 → current max limit 1.13 mA/V.
- HSE sense amplifier threshold (HSES = RCC_HSECR[3]) is set to 0 → HSE bias current factor 1/2

2.2.2 Software implementation

Project configurations

Two project configurations are available in the package:

1. One for the calibration procedure (determination called STM32WBxx_Nucleo_Set_Calibration)
2. One to test the stored value (called STM32WBxx_Nucleo_Test_Calibration). This last configuration is given as an implementation example of the HSE clock initialization in RF applications.

The firmware is built on the STM32WB HAL drivers.

1. STM32WBxx_Nucleo_Set_Calibration:

The device is programmed to:

- Send the HSE clock on the PA8 pin.
- Modify and set the load capacitance value when push-buttons SW1 and SW3 are actioned.
- Store the load capacitance value together with the 48 bits of additional data (Bluetooth device address) in the OTP or the selected Flash area.

2. STM32WBxx_Nucleo_Test_Calibration

This configuration is for testing the actual HSE setting:

- Configure the HSE clock and output it on PA8 pin
- Fetch the load capacitance value from the OTP/Flash area
- Program HSE_CFG register accordingly

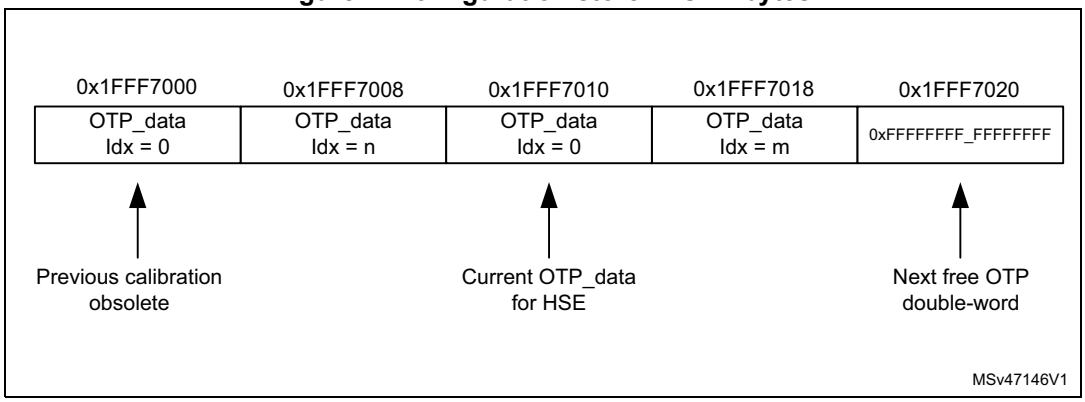
Storage in One-Time-Programming bytes (OTP)

Load capacitance value is included in a 64 bits structure. Each OTP structure type is indicated by its index (one byte). The index used for the structure in this application note is 0. Six bytes remain to store additional data like MAC, Bluetooth device address or crypto key.

```
typedef __packed struct
  {
    uint8_t   additional _data[6]; /* 48 bits */
    uint8_t   hse_tuning; /* Load capacitance value */
    uint8_t   index; /* structure index ==0x00*/
  } OTP_BT_t;
```

Even if the configuration phase is not supposed to be repeated, there may be some case where it should be overwritten. When using OTP bytes current configuration cannot be removed, the new one is placed at the next free double-word slot (see *Figure 7*).

Figure 7. Configuration store in OTP bytes



When the calibration phase has been done, the application initialization phase must retrieve the load capacitance (and other additional data) from this OTP area. The value retained is then the last one with the right index.

2.2.3 Scripts

Two batch scripts are provided to run each FW configuration:

- STM32WBxx_Nucleo_Set_HSE_Calibration_OTP.bat
- STM32WBxx_Nucleo_Test_HSE_Calibration_OTP.bat

These scripts call the ST-Link Utility in command-line mode, and the path to the tool shall be set accordingly:

- SET STLINK="~ \STM32 ST-LINK Utility\ST-LINK Utility\ST-LINK_CLI.exe"

The binary or hex file of the configuration shall be set also

1. For Keil®:

- SET HEXFILE="MDK-ARM_CM4\STM32WBxx_Nucleo\STM32WBxx_Nucleo_Set_Calibration.hex"

2. For IAR™:

- SET EXFILE="EWARM\STM32WBxx_Nucleo_Set_Calibration\Exe\STM32WBxx_Nucleo_Set_Calibration.hex"

3. For SW4STM32:

- SET HEXFILE="STM32WBxx_Nucleo_Set_Calibration\Debug\STM32WBxx_Nucleo_Set_Calibration.hex"

The 48 bits of additional data (in bold in next command) are transmitted to the device through these scripts. They are stored inside the SRAM and read by the FW.

*STLINK_CLI.exe -c swd -w64 0x2002FFF0 0X0000**112233445566***

3 Conclusion

RF applications require a very accurate clock, to ensure best performance. The RF clock is derived from an external 32 MHz crystal, and the frequency fine tuning is obtained by setting the right load capacitance at crystal pins.

STM32WB Series introduces a very efficient architecture with internal capacitances setting, removing the need of extra component on PCB, and lightening the constraints on the crystal performance.

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
27-Sep-2017	1	Initial release.
14-Nov-2017	2	Updated: – *Section 2.2.2: Software implementation* – *Section 2.2.3: Scripts*
21-Feb-2019	3	Changed document classification, from ST restricted to Public. Updated *Section 1: STM32WB Series HSE oscillator*. Minor text edits across the whole document.