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Revision: 6

SpeedFit User Manual

1. Introduction

SpeedFit is a powerful tool for the selection and comparison of Wolfspeed's SiC semiconductor devices in common circuit topologies. The user is able to input realistic system parameters related to their application of interest and virtually test components to estimate losses and expected temperature of the devices in a given application.

The SpeedFit user interface consists of a set of seven tabs to guide the user towards an end goal of simulated current and voltage waveforms and performance data. This data will allow the user to quickly quantify the advantage of Wolfspeed devices in the application of interest.

2. Application and Input tab

The first step is to select the appropriate topology to simulate. The first tab, **[Application]**, has the user select the type of converter system based on the input and output form of electrical power. Broad categories include DC/DC, AC/DC and DC/AC with both single- and three-phase options in the last 2 categories as shown in Figure 1. Use the **<Next>** button to proceed to the next tab. The table below describes each on the input parameters encountered on the **[Input]** tab.

Figure 1: Application Tab

Topology	Input Parameters (Units)	Description
DC/DC ➢ **Buck** ➢ **Boost** ➢ **Buck-boost** ➢ **3-level boost**	Input voltage (VDC)	Input DC supply to the converter and the range limit is 10 V < V_i < 1700 V
	Output voltage (VDC)	Output DC voltage from the converter and the range limit is 10 V < V_o < 1700 V
	Rated output power (W)	Output power rating of the converter and the range limit is 100 W < S_o < 300 kW
	Switching frequency (kHz)	MOSFET gate pulse signal frequency and the range limit is 1 kHz < F_{sw} < 500 kHz
DC/DC ➢ **LLC resonant converter***** ➢ **Phase shift full bridge** ➢ **Bi-directional CLLC*****	Input voltage (VDC)	Input DC supply to the converter and the range limit is 100 V < V_i < 1700 V for LLC/CLLC; 250 V < V_i < 850 V for Phase shift full bridge.
	Output voltage (VDC)	Output DC voltage from the converter and the range limit is 100 V < V_o < 1700 V for LLC/CLLC; 250 V < V_o < 750 V for Phase shift full bridge.
	Rated output power (W)	Output power rating of the converter and the range limit is 100 W < S_o < 300 kW for LLC/CLLC; 2kW < S_0 < 100kW for Phase shift full bridge.
	Switching frequency (kHz) & Dead time (ns)	MOSFET gate pulse signal frequency and the range limit are 10 kHz < F_{sw} < 1000 kHz for LLC/CLLC; 50 kHz < F_{sw} < 500 kHz for Phase shift full bridge. Max dead time is equal to 15% of t_{sw}
AC/DC* ➢ **1ph 2-Level AFE** ➢ **3ph 2-Level AFE** ➢ **1ph 3-Level NPC AFE** ➢ **3ph 3-Level NPC AFE** ➢ **3ph 3-Level T-type AFE** ➢ **Totempole converter** ➢ **3ph Vienna rectifier**	Input voltage (Vrms,l-l)	Input AC supply to the converter and the range limit is 10 V < V_i < 1700 V
	Output voltage (VDC)	Output voltage from the converter and the range limit is 10 V < V_o < 1700 V
	Rated output power (W)	Output power rating of the converter and the range limit is 100 W < S_o < 300 kW

➢ **Bridgeless PFC boost rectifier****	Switching frequency (kHz) & Dead time (ns)	MOSFET gate pulse signal frequency and the range limit is 1 kHz < F_{sw} < 500 kHz Max dead time is equal to 15% of t_{sw}
	AC frequency (Hz)	Input supply line frequency range is 40 < f_{line} < 250Hz
DC/AC* ➢ **1ph 2-Level inverter** ➢ **3ph 2-Level inverter** ➢ **1ph 3-Level NPC inverter** ➢ **3ph 3-Level NPC inverter** ➢ **3ph 3-Level T-type inverter**	Input voltage (VDC)	Input DC supply to the inverter and the range limit is 10 V < V_i < 1700 V
	Output voltage (Vrms,l-l)	Output AC voltage from the inverter and the range limit is 10 V < V_o < 1700 V
	Power factor	0.5 < pf <1
	Rated output power (VA)	Output power rating of the converter and the range limit is 100 W < S_o < 300 kW
	Switching frequency (kHz) & Dead time (ns)	MOSFET gate pulse signal frequency and the range limit is 1 kHz < F_{sw} < 500 kHz Max dead time is equal to 15% of t_{sw}
	AC frequency (Hz)	Inverter output frequency range is 40 < f_o < 250Hz

Table 1: Input tab parameters and their descriptions.

* Operating criteria: 1ph => V_{in} > sqrt(2)*V_{out}; 3ph => V_{in} > sqrt(2/3)*2*V_{out};

** Total diode losses excluded losses of Bypass diode.

*** Refer to Appendix A for additional information about LLC/CLLC topologies.

The Input tab has the user specify system level parameters for input and output voltage, the rated output power, and the switching frequency. The suitable topologies available will be auto-filtered based on this output voltage value and its relation to the input voltage. For example, when the input voltage value is higher than the output voltage value, both the buck converter and buck-boost converter will be available to select, but not the boost converter, as shown in Figure 2.

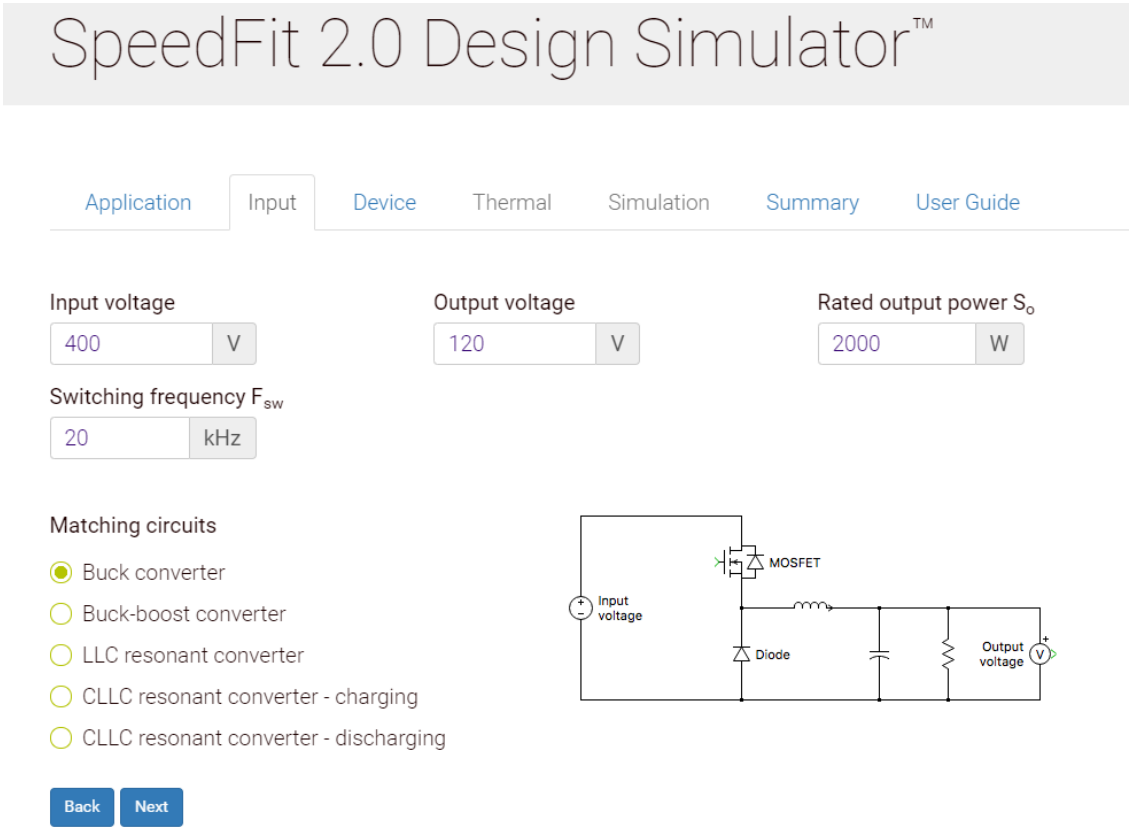

Figure 2: Input Tab

3. Device Selection Tab

The Device tab has the user select the power devices for their converter. By default, the tool will provide a set of recommended device options based on power the user input, but a full list of MOSFETs and Modules can be shown by clicking the **<Show all>** button at the top of each list. The parts that are available for simulation have a radio button in the first column.

For DC/DC applications, both MOSFET and diode selection must be made. Only a MOSFET or Module can be selected for AC/DC and DC/AC applications. External Schottky diodes can also be added in parallel to discrete MOSFETs for AC/DC and DC/AC applications to reduce switching losses. Modules, by default, have Schottky diodes built in. Once a part has been selected the user can then select the number of devices to be paralleled to make up a single functional switch. The user can then change the default gate resistance for turn-on and turn-off for all MOSFET and Module devices. The gate resistance controls the switching speed of the device and has significant impact on switching losses.

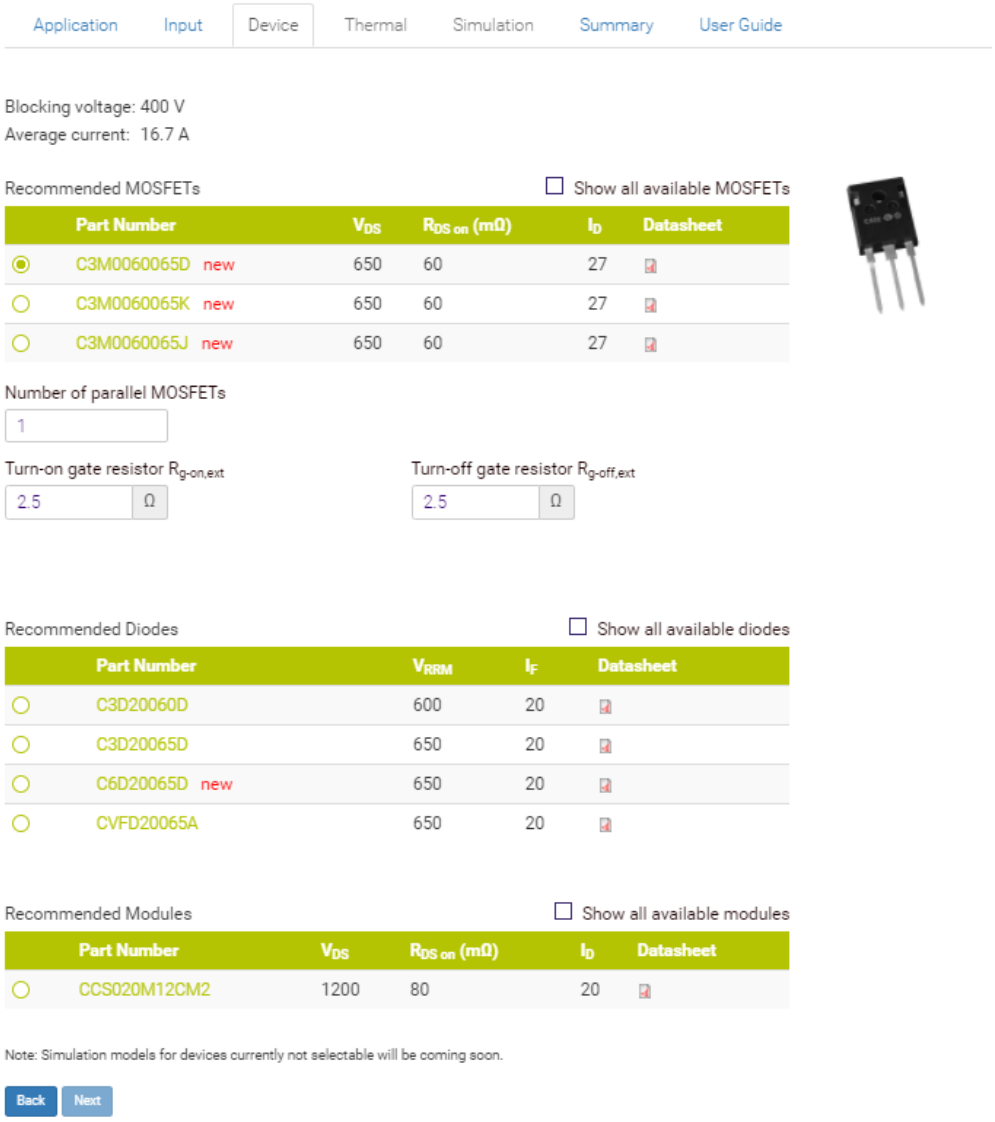

Figure 3: Device Tab

4. Thermal Tab

This tab has the user defining the cooling system thermal properties for their converter. The cooling system has all devices mounted on a common heatsink. The thermal interface resistance between the case of each device and the corresponding heatsink is then specified, with a possible range of 0 K/W < $R_{th,ch}$ < 10 K/W.

Next, the user has two options for the simulation of the thermal system; either the heatsink temperature can vary throughout the simulation or fixed with a specific value. If the heatsink temperature is variable, the thermal resistance between the heatsink and ambient environment, heatsink time constant and ambient temperature must be defined. User has an option to couple an additional heat source, such as an auxiliary converter to a common heatsink.

The following parameter range limits:
0 K/W < $R_{th,ch}$ < 20 K/W
0 s < τ_{ha} < 100 s
-50 °C < T_{amb} < 150 °C
0 W < P_{add} < 2000 W

When a fixed heatsink temperature simulation is defined, the temperature is defined with a possible range of -50 °C < T_h < 150 °C.

Below are some references about typical thermal interface resistance values:

Thermal Interface	**Typical value of R_{cs} (°C/W)**
To247 - Thermal Grease (non-isolated)	0.22
TO247 - Thermal Grease w/ 0.5mm ceramic tile isolation	0.6
62mm Module	0.02
45mm Module	0.03
Heatsink	**Typical value of R_{sa} (°C/W)**
Air cooling	
LFM	
100	0.757
200	0.536
300	0.439
400	0.378
500	0.338
600	0.309
700	0.286
800	0.268
900	0.252
1000	0.239
Liquid Cooling	
Liquid cooling – Pin fin style heatsink with 1 GPM flow	0.05 - 0.12
Cold plate	0.15 - 0.25

Table 2: Typical thermal interface resistance values

*Note that the $R_{th,ch}$ value is always defined for each switch position. Therefore, when using Modules, the user should multiply their intended $R_{th,ch}$ value by the number of switch positions. For half-bridges with two switch positions, the user should enter a value of 2 * their desired $R_{th,ch}$ value, and for six-packs with six switch positions, the user should enter a value of 6 * their desired $R_{th,ch}$ value. These gain factors are required to ensure that a reduction in equivalent thermal resistance due to the parallel connections in the model is mitigated. No gain factors are required for $R_{th,ch}$ when using discrete devices.

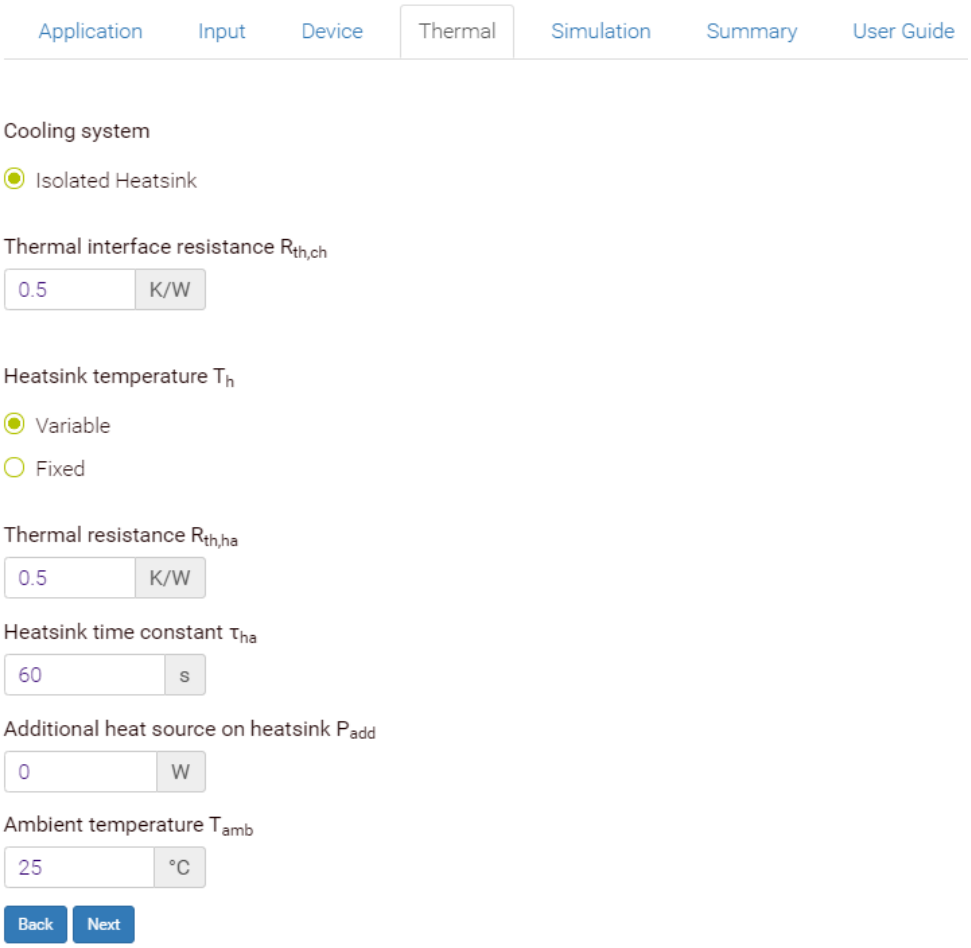

Figure 4: Thermal Tab

5. Simulation Tab

The Simulation tab has the user run system simulations with the defined parameters and configurations and display the simulated waveforms and tabular result data.

The circuit model is displayed showing the topology, heatsink configuration, and key parameter values specified by the user. Depending on the circuit type, some passive component parameters such as inductance and capacitance can be tuned by the user at this stage before pressing the **<Simulate>** button.

A simulation is executed by clicking the **<Simulate>** button below the circuit schematic and data tables. A steady-state simulation of the system is then performed, and several cycles of the input/output voltage and current waveforms are displayed for this equilibrium condition.

The scopes can be reordered vertically by dragging on the title bars and resized using the arrows at the bottom right corners. Each scope has a set of data cursors that can be enabled by clicking on the **<Cursors>** button at the top. This allows the user to perform measurements of time, voltage and current values.

The System overview results table displays the input voltage, rated output power, switching frequency, and efficiency for the system. The Device overview results table displays the total switching, conduction, and combined losses for all MOSFETs, modules, and diodes in the circuit. The total converter losses are displayed, which is the sum of these individual totals. The junction temperatures of the MOSFETs, modules, and diodes are also displayed.

The user can save the simulated waveforms and results data by clicking the **<Hold result>** button to the right of the **<Simulate>** button. A Result History list will then appear below the result tables, where each simulation trace is listed. This allows for changing of system or component parameter values, devices, thermal configurations, etc., and comparing the results in subsequent simulations. To modify any part of the system setup once at the Simulation tab, the user can navigate directly to the desired tab at the top of the tool or use the Back and Next buttons. Note that while all combinations of configurations can be compared with the resultant data and waveforms presented, changing the circuit type will only show the active schematic. Comparing simulations using different converter types and displaying all historical traces is not recommended as the resultant waveforms may require different display scales.

A simulation trace can be held by clicking the green <+> button and removed by clicking the red <-> button. Each trace name can be renamed by clicking on the respective text field. Traces can also be displayed and hidden by using the check boxes to the left of the trace name. This allows user to compare the current and other traces' results using the same table and measurement of the scope (Figure 5). New simulation traces will always appear at the top of the Results History list and each data table field.

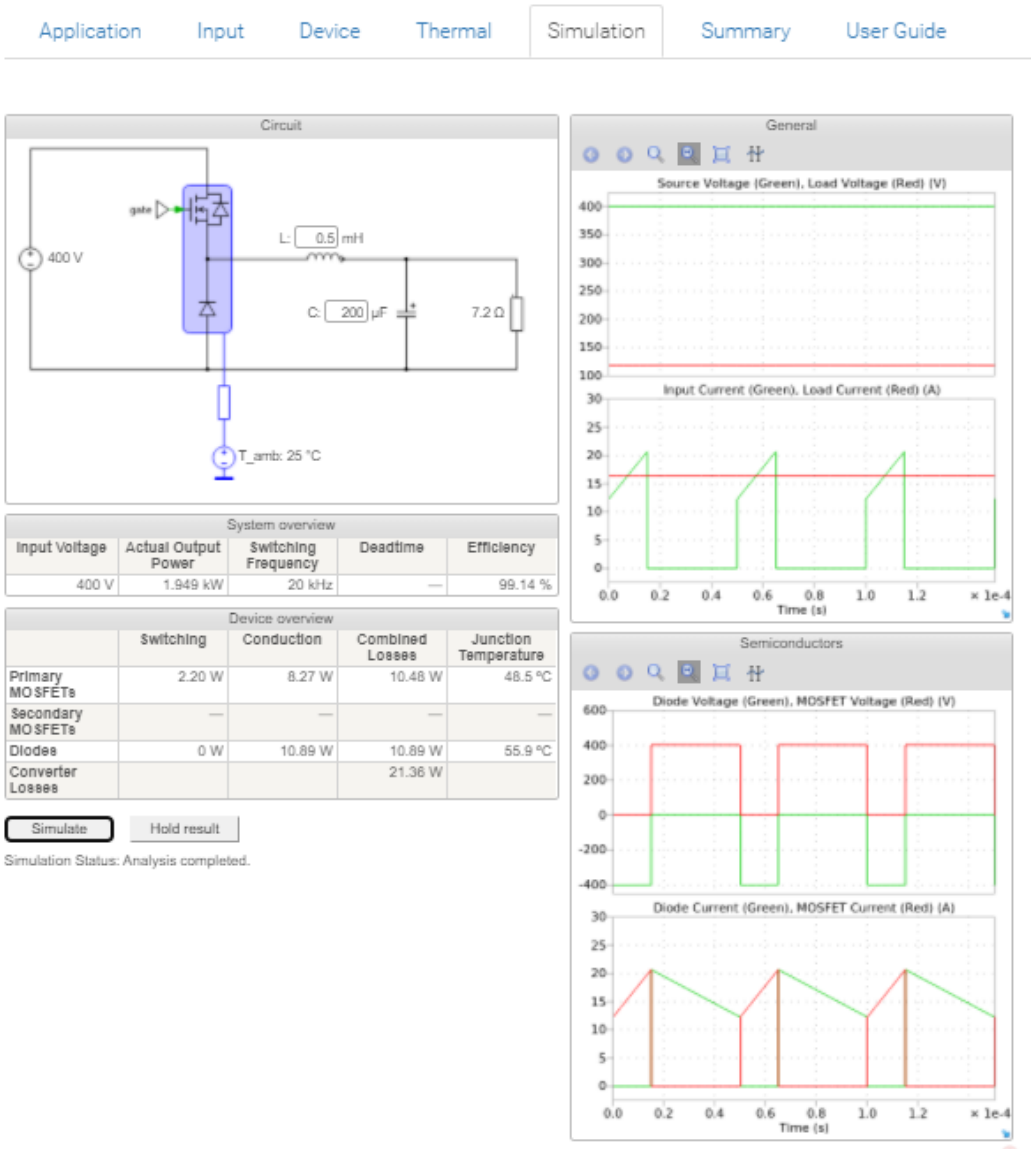

Figure 5: Simulation Tab

6. Summary Tab

The Summary tab displays the system parameters, Wolfspeed device part number and simulation results in one glance. Each variant represents the individual saved simulation. Information on this page can be saved or printed by pressing the “Print” button. The “Request Sample” button will allow the user to request component samples directly from SpeedFit online simulation tool. If you want a sales representative to call you, press the “I would like a sales representative to call me” button.

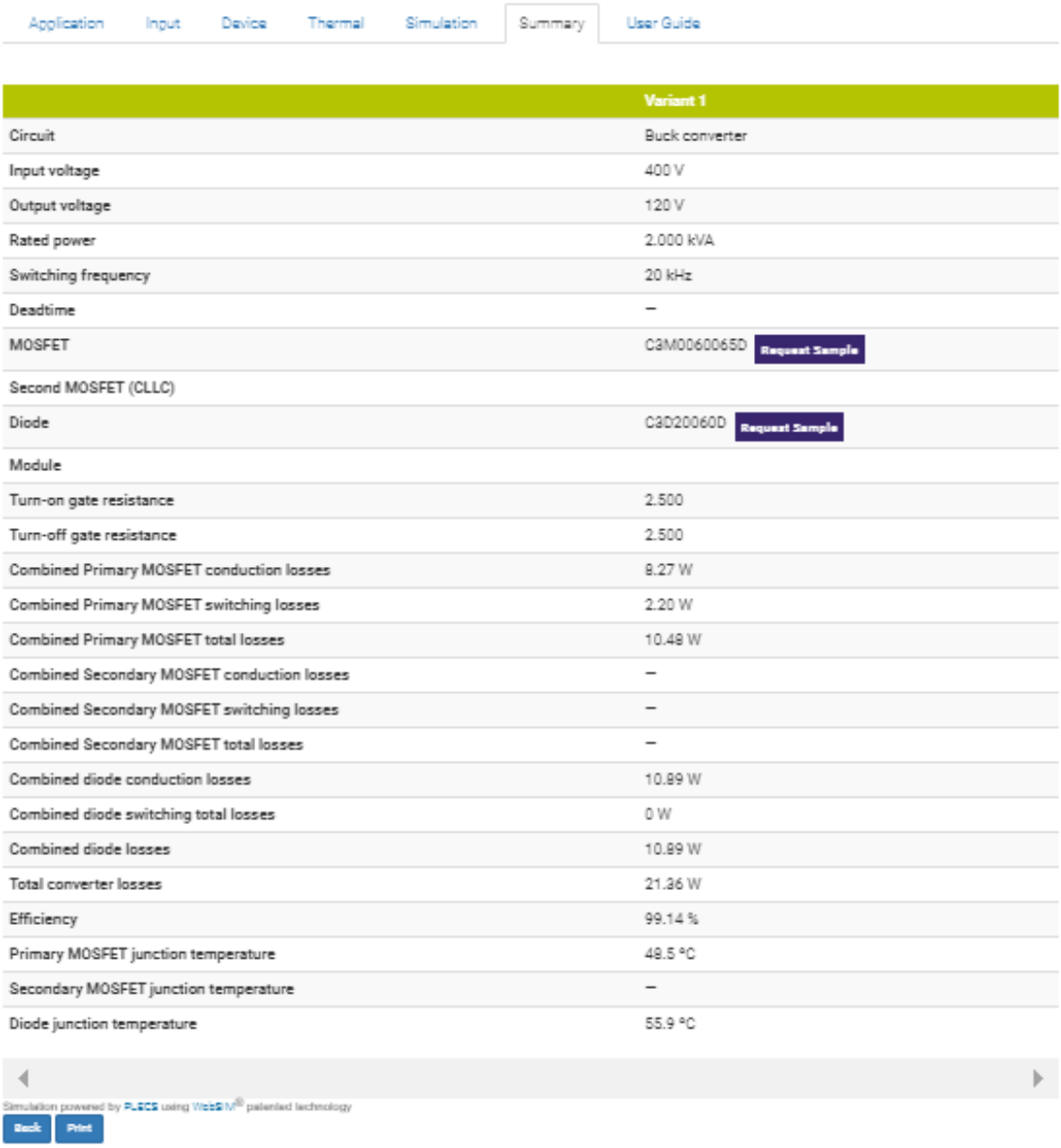

Figure 6: Summary Tab

7. User Guide Tab

This is the tab where you can download the SpeedFit online simulator user manual.

Appendix A

New features for the LLC and CLLC topologies have been added to SpeedFit. Due to the flexibility of the converters, some users may find the parameterization process confusing. Once the system **nominal** parameter set has been entered, users can click the "Cr & Lr" button to have SpeedFit propose the C_r and L_r values. The proposed resonant tank of the LLC/CLLC has been optimized to provide good performance over a broad operating range. If the proposed values do not meet the user's requirements, the user can change these values by entering their own C_r value and after that clicking the "Lr" button.

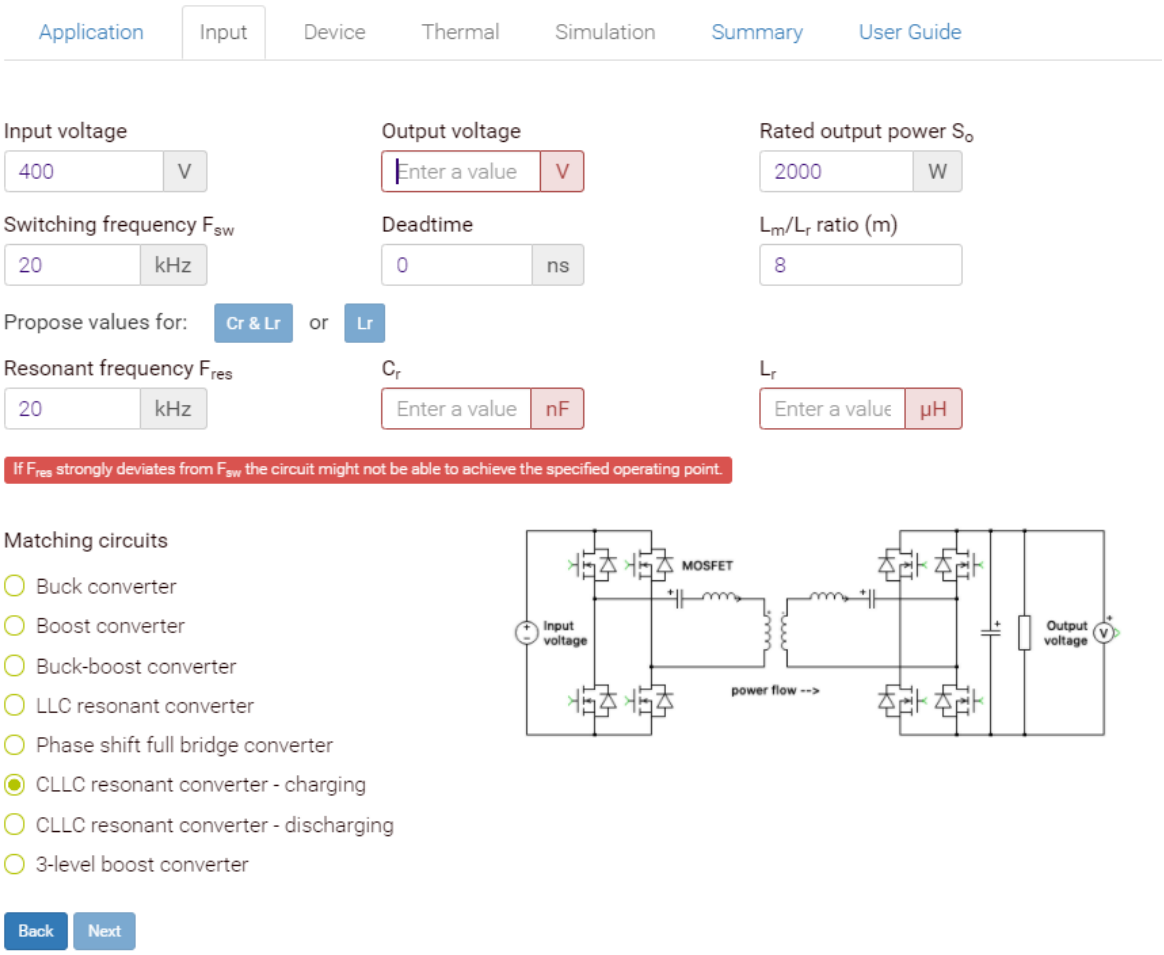

Figure 7: Input Tab with CLLC resonant converter charging mode selected

Once the C_r and L_r values are proposed, the turn ratio of the transformer is fixed. The user can simulate these converters with different V_{in}, f_{sw}, deadtime and S_o conditions. This feature enables the user to obtain the losses for different conditions. To start over with a new requirement, the user just needs to enter the new system specification and then click the "Lr & Cr" or "Lr" button again. To optimize the efficiency of the converter, L_m is by default $12*L_r$ for the LLC and $8*L_{r\_pri}$ for the CLLCs.

Deadtime is added to make sure one switch is fully turned off before the complementary switch is turned on. If the deadtime period is too long, then it can cause a voltage dip and switches are switching at non ZVS (as shown in Figure 8). Due to fact that PLECS treats all switches as ideal, there is no C_{oss} capacitance, and no snubber capacitor has been included in the circuit. In the case that the desired deadtime creates this voltage dip behavior, the user can change the L_m value by lowering the ratio of L_m/L_r (m) to overcome the issue. If the user needs to maintain a higher m value, then reducing the L_r value directly can also solve this problem.

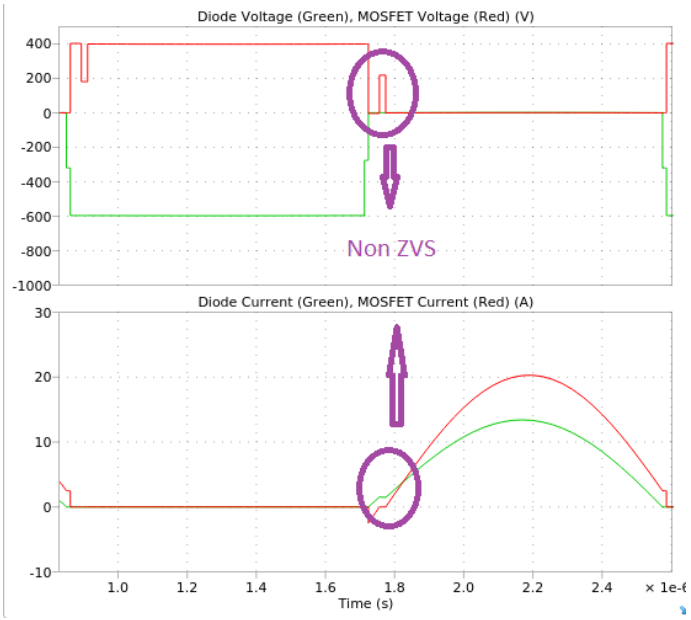

Figure 8: Non ZVS when dead time duration is too long

The user can adjust the switching frequency (F_{sw}) to increase or decrease the output voltage (V_o) (as shown in Figure 9). If the resonant frequency (F_{res}) strongly deviates from F_{sw}, the circuit might not be able to achieve the specified operating point. So, it is recommended not to increase or decrease F_{sw} too much from F_{res}. By decreasing the value of F_{sw} until the point where V_o starts reducing instead of increasing, the converter is falling into the capacitive region and V_o will continue reducing if F_{sw} is further decreased (as shown in Figure 10).

The bi-directional CLLC converter has two operating modes, which are charging and discharging mode. During charging mode, the power is delivered from the primary to secondary side. For discharging mode, the power flows in the reverse direction, from the secondary to primary side. The LLC and CLLC converters are operated in open-loop fashion; thus, if the V_{in} or S_o values are changed, the user needs to adjust the value of F_{sw} to regulate V_o.

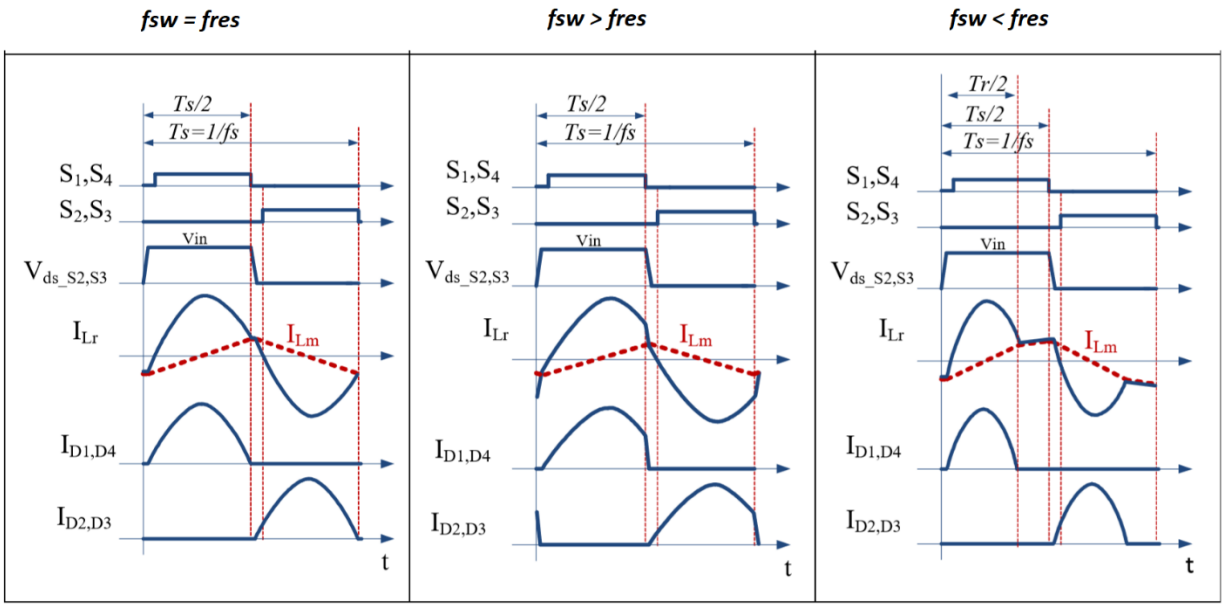

Figure 9: LLC/CLLC waveforms

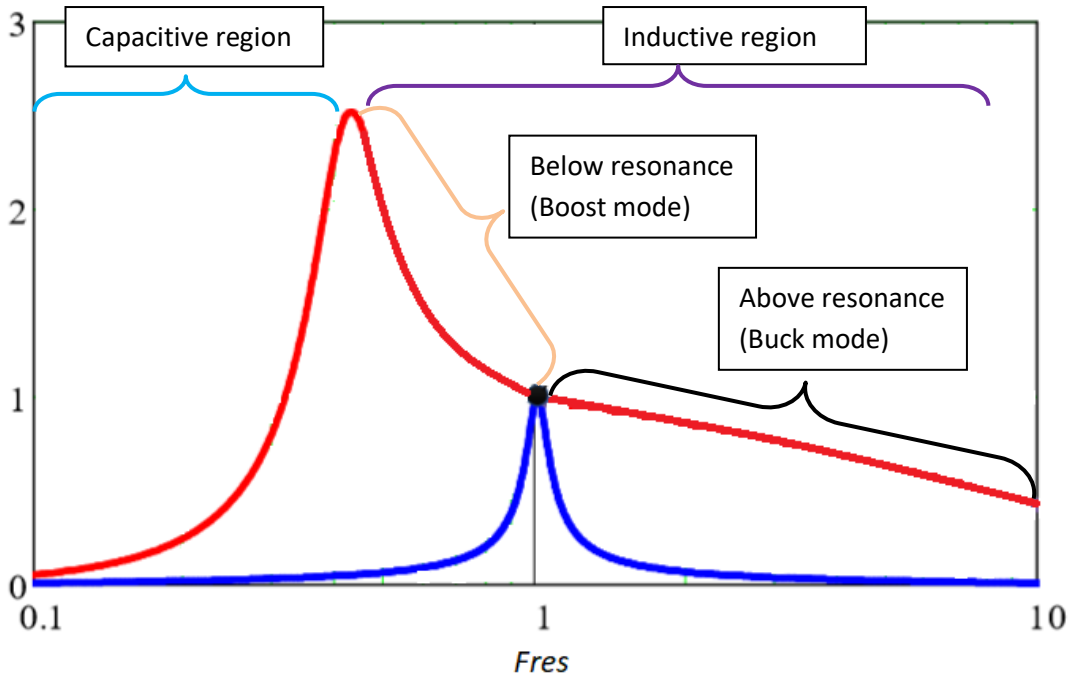

Figure 10: LLC/CLLC modes and regions of operation